Recommended Usage of IPSiLog Serial SRAM products

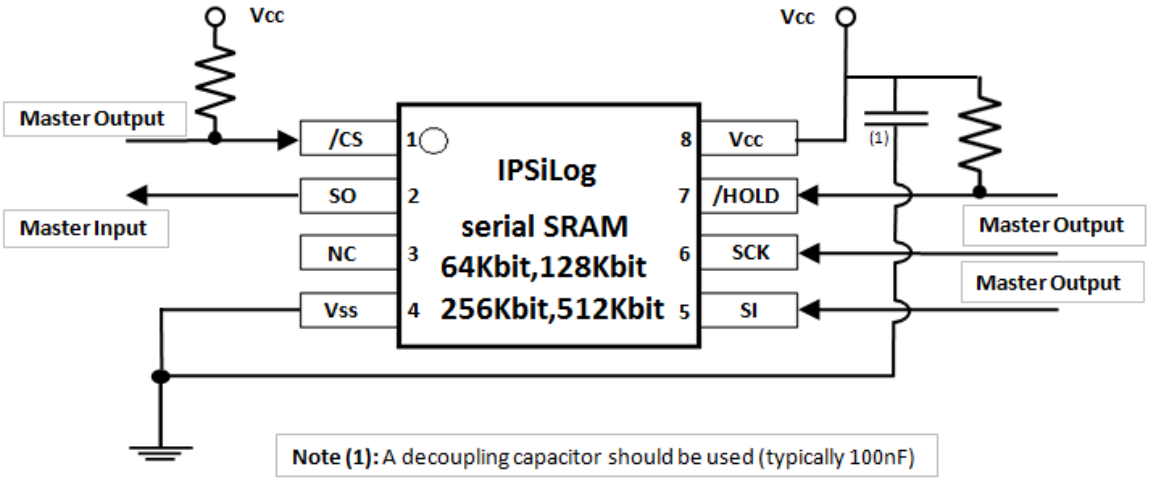
OVERVIEW

The serial SRAM family of IPSiLog products offers the customer serial high speed, low power, standalone SRAM memory at writing speeds up to 20MHz at various densities starting at 64Kbit. They are an alternative choice to the traditional parallel architecture that saves both board area and also I/O count on the MCU.
These devices employ an industry standard 4-wire synchronous SPI interface that can easily be connected to a microcontroller with SPI-Interface or using GPIO pins. A clock SCK is used to latch data into and out of the device, and a chip select pin is used to enable/disable the device.
For microcontroller-based systems that require high serial data rates, the SPI interface is an ideal choice.
A dedicated SPI port on a microcontroller makes the choice an easy one in those cases. However, many microcontrollers do not have a dedicated SPI port, so the use of bit-banging provides a means to use general purpose I/O pins. This method involves software that controls the I/O port.

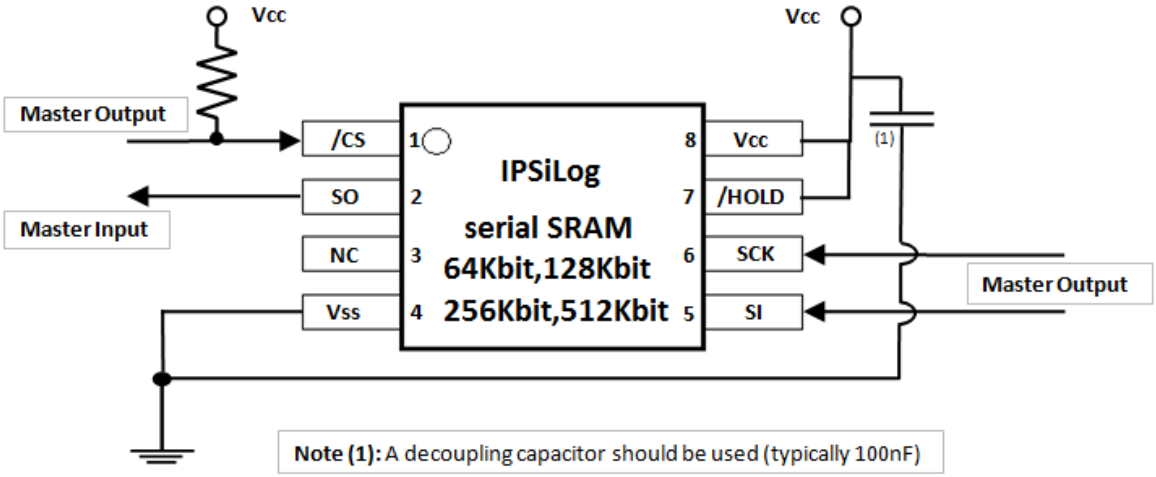
The IPSiLog serial SRAM is supporting two SPI-Modes: SPI-Mode 0 (CPOL:0, CPHA:0) and SPI-Mode 3 (CPOL:1, CPHA:1). In both Modes data are clocked into the device on the rising SCK edge and clocked out on the falling edge of SCK. The difference between Modes 0 and 3 is simply whether SCK starts low or high when /CS is asserted low.

Recommended Connection of IPS12xxxxx devices

With /HOLD function



Without /HOLD function



If the HOLD function is not needed, the HOLD pin can be tied to V_{CC} to save a microcontroller pin. Its never good practice leaving an input pin floating.

To protect the SRAM from corrupting data during power cycles, we recommend that the /CS and /HOLD pins are held inactive as V_{SS} powers up and powers down. In many cases, this may be as simple as a pullup resistor on the MCU's output pin that drives /CS and /HOLD.

To filter out small ripples on V_{SS}, a decoupling capacitor (typically 100nF) should be put between V_{CC} and GND close to the V_{CC} pin. This is strongly recommended to connect the decoupling capacitor if V_{CC} is noisy and/or the serial SRAM is used at high frequency in sequential mode.

POWER CYCLING

Care must be taken in controlling signals during power cycle events. It is important to understand the device might inadvertently write data at mid-level power supply levels when chip select is active (low), for example. The system designer should be aware of chip-enable and V_{CC} states during power cycles.
It is the user's responsibility to ensure that V_{CC} is within datasheet tolerances to prevent incorrect operation. It is recommended that the V_{CC} power supply voltage ramp up from 0V to Vcc straightly and ramp down from Vcc to 0V in a well-controlled manner. V_{CC} should not linger at an ambiguous level. MCU and serial SRAM should always reset together by bringing the serial SRAM to 0V before returning to normal operating level. It is recommended to initialize the whole memory-array by writing "0" to all addresses, before usage.

SYSTEM HOOKUP

Multiple devices may be used as long as the controller has extra pins to drive a chip select /CS to each SRAM device. If the HOLD function is not needed, the HOLD pin can be tied to V_{CC} to save a microcontroller pin.

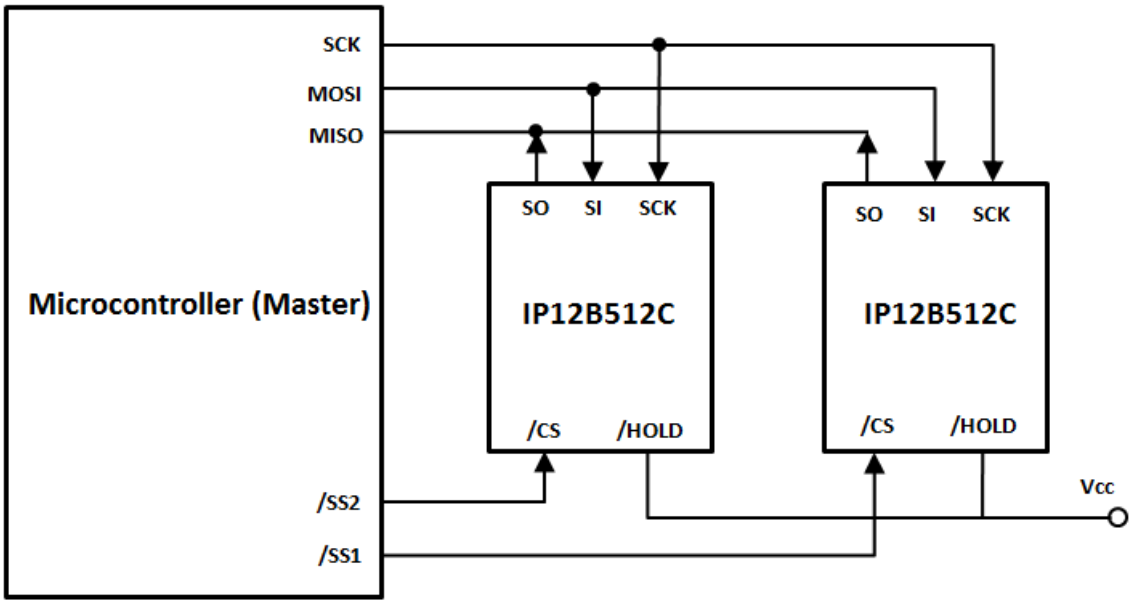


Figure 3. System Configuration for two serial SRAM Devices (simplified schematic)

For a microcontroller that has no dedicated SPI bus, a general purpose port may be used.